

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:

Kinsman et al.

Serial No.: 10/624,833

Filed: July 22, 2003

For: METHOD FOR FABRICATING A
CHIP SCALE PACKAGE USING WAFER
LEVEL PROCESSING (as amended)

Confirmation No.: 6568

Examiner: M. Estrada

Group Art Unit: 2823

Attorney Docket No.: 2269-3572.2US
(97-1243.02/US)

Notice of Allowance Mailed:

November 19, 2004

Express Mail Mailing Label No.: EL 994826070 US

Date of Deposit with USPS: February 15, 2005

Person making Deposit: Steve Wong

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

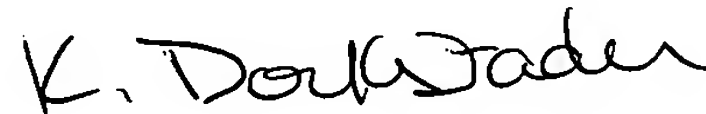
Applicants submit herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of \$1,715.00 in payment therefor plus five (5) copies of the patent when issued.

Also, enclosed is an Amendment Pursuant to 37 C.F.R. § 1.312(a) (12 pages), plus attached Replacement Sheets of Drawings (2 sheets) and Annotated Sheets Showing Changes

Made (2 sheets); Comments on Statement of Reasons for Allowance (2 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Applicants understand that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,

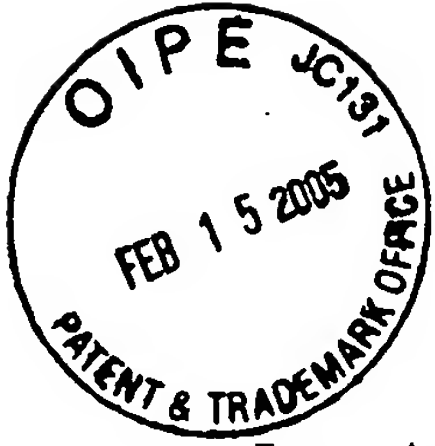


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Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: February 15, 2005
KLD/ps:dd

Enclosures: Part B - Issue Fee Transmittal
Check No. 21361 in the amount of \$1,715.00
Copy of Transmittal Letter
Amendment Pursuant to 37 C.F.R. § 1.312(a) (12 pages), plus attached
Replacement Sheets of Drawings (2 sheets) and Annotated Sheets
Showing Changes Made (2 sheets)
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Document in ProLaw



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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

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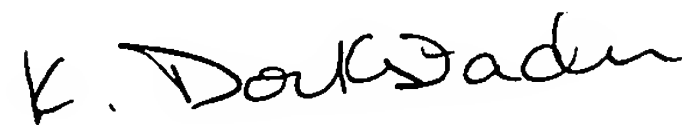
The Examiner indicates:

[T]here is no disclosure in the prior art of forming a pattern of mutually transverse channels in the active surface to a depth below the at least one layer of integrated circuit, the channels circumscribing a semiconductor device location comprised of at least one individual die and exposing peripheral edges of the at least one layer of integrated circuitry; applying an encapsulant material at least over the active

surface and into the channels to a depth exceeding the height of projection of the intermediate conductive elements; and placing the semiconductor substrate with the intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate.

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Applicants respectfully submit that independent claim 1 recites, "forming a pattern of mutually transverse channels in the active surface to a depth below the at least one layer of integrated *circuitry*." (emphasis added) Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,



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